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POWER SUPPLY CLAMP CIRCUIT

Abstract

A power supply clamp circuit for preventing damage to an integrated circuit due to electrostatic discharge. The power supply clamp circuit includes a voltage generator electrically connected to a first node for generating a voltage; a first PMOS transistor having a source electrically connected to the first voltage source, a gate electrically connected to the first node, and a drain electrically connected to a second node; a first NMOS transistor having a drain electrically connected to the second node, a gate electrically connected to the first node, and a source connected to ground; a second NMOS transistor having a drain electrically connected to the first voltage source, a gate electrically connected to the second node, and a source connected to ground; and a second PMOS transistor having a source electrically connected to the second node, a gate and a drain commonly electrically connected to the first node.